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September 7, 2000

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Sir:

Transmitted herewith for filing is the Patent Application of:

Inventor(s): **Anthony M. Chiu**

For: **SURFACE MOUNT PACKAGE WITH INTEGRAL ELECTRO-STATIC CHARGE DISSIPATING RING USING LEAD FRAME AS ESD DEVICE**

Enclosed are:

jc511 U.S. PTO 09/656984 09/07/00

X Patent Specification and Declaration

X 7 sheets of drawing(s).

X An assignment of the invention to STMicroelectronics, Inc. (includes Recordation Form Cover Sheet).

__ A certified copy of a __ application.

__ Information Disclosure Statement, PTO 1449 and copies of references.

The filing fee has been calculated as shown below:

For	Number Filed	Number Extra	Rate	Fee
Basic Fee				$690.00
Total Claims	20 - 20	0	x 18 =	$ .00
Indep. Claims	4 - 3	1	x 78 =	$ 78.00
MULTIPLE DEPENDENT CLAIM PRESENTED			x 260 =	$
			TOTAL	$768.00

X Enclosed please find our checks in the amounts of $768.00 and $40.00.

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X Any additional filing fees required under 37 CFR §1.16.

X Any patent application processing fees under 37 CFR §1.17.

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Respectfully submitted,

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S P E C I F I C A T I O N

Docket No. 00-C-016

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN that I, Anthony M. Chiu, a citizen of the United States of America residing in the State of Texas, have invented new and useful improvements in a

SURFACE MOUNT PACKAGE WITH INTEGRAL ELECTRO-STATIC CHARGE DISSIPATING RING USING LEAD FRAME AS ESD DEVICE

of which the following is a specification:

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates generally to packaging integrated circuit devices and in particular to providing electrical discharge properties to integrated circuit device packaging. Still more particularly, the present invention relates to forming a metal ring an integrated circuit from a portion of a lead frame for the purpose of conducting electrostatic energy away from the integrated circuit.

2. Description of the Prior Art:

In conventional integrated circuits, electrostatic discharge (ESD) events typically enter the circuitry through the pad ring, which dissipates the charge before reaching the core. Some recently developed integrated circuits, however, must necessarily expose the core of the circuitry to ESD events. Contemporary fingerprint sensors, for example, often include a two-dimensional array of sensing electrodes proximate to a sensing surface on which the finger is placed, with ridges and valleys on the finger skin detected by capacitance variations caused by the varying distance between the skin surface and the sensor electrodes. The need for contact with the finger in order to detect fingerprint features necessitates exposure of the integrated circuit to electrostatic discharge events resulting from a finger touching the sensing surface.

The electrostatic charge which may be carried by a human body oftens fall within the range of several kilovolts or more. Typical electrostatic discharge protection circuits

have proven somewhat ineffective in safely dissipating such charges, which may provide sufficient energy to break through upper dielectric/passivation layer.

Additionally, integrated circuits which cannot be completely encapsulated--except for conductive leads to the circuit--during packaging (e.g., fingerprint sensors, optical sensors, and other circuit requiring that a portion of the integrated circuit remain exposed) are typically mounted utilizing "Chip On Board" technology. The integrated circuits are mounted on a printed circuit board in an unencapsulated form, connected to the printed circuit board through the bond wires, then protected utilizing liquid encapsulation or silicon gel. Such mounting, which involves the use of gold plating of the substrate, is much more expensive than conventional surface mounting of integrated circuits on a stamped lead frame. However, viable surface mounting of fingerprint sensors on lead frames has not yet been achieved.

It would be desirable, therefore, to provide a technique for surface mounting of fingerprint sensors on lead frames while providing adequate electrostatic discharge protection to the packaged integrated circuit.

SUMMARY OF THE INVENTION

In a packaged integrated circuit, electrostatic discharge protection is provided by portions of a lead frame on which the integrated circuit is mounted. The lead frame includes a die paddle on which an integrated circuit die is mounted, with plastic or epoxy material encapsulating exposed surfaces of the integrated circuit die except for a sensing surface, and supporting pins or leads formed from the lead frame. Portions of the lead frame extending from the die paddle are folded around sides of the encapsulated integrated circuit die and over, or adjacent to and level with, a peripheral upper surface of the encapsulated integrated circuit die to form an electrostatic discharge ring. The lead frame portions folded around the integrated circuit package are connected to ground through a ground pin, so that charge on a human finger touching the electrostatic discharge ring is dissipated to ground before the finger contacts a sensing surface of the integrated circuit. The portions of the lead frame which are folded around the encapsulated integrated circuit die may extend only around sides or side regions of the integrated circuit package not including pins or leads or, alternatively, may extend around all sides of the integrated circuit package and have openings where side regions of the integrated circuit package includes pins or leads.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figures 1A-1E depict various views of a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention;

Figures 2A-2D are various views of alternative designs for a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention;

Figures 3A-3B depict plan views of lead frame strips utilized in forming a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention; and

Figures 4A-4C are various views of a narrow-strip packaged integrated circuit with gull-wing leads and an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION

The following description details the structure, application and features of the present invention, but it will be understood by those of skill in the art that the scope of the invention is defined only by the issued claims, and not by any description herein. The process steps and structures described below do not form a complete process flow for manufacturing integrated circuit packages. The present invention can be practiced in conjunction with integrated circuit package fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures showing portions of an integrated circuit package during fabrication are not necessarily drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

With reference now to the figures, and in particular with reference to **Figures 1A** through **1E**, various views of a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from a lead frame portion in accordance with a preferred embodiment of the present invention are depicted. **Figure 1A** depicts a plan view of the integrated circuit package **102**, while **Figure 1B** depicts a side view, **Figure 1C** depicts a cross-sectional view taken at section lines **A-A**, **Figure 1D** depicts a back or bottom view, and **Figure 1E** depicts an isometric view. Packaged integrated circuit **102** in the exemplary embodiment includes an fingerprint sensor integrated circuit die **104** having a sensing surface **106** proximate to an array of sensor electrodes. A finger is placed on sensing surface **106** of packaged integrated

circuit **102** in order to detect the fingerprint; accordingly, sensing surface **106** must remain exposed and should not be encapsulated.

Integrated circuit die **104** is mounted on a stamped metal lead frame **108**, affixed to lead frame **108** by an adhesive **110**. A peripheral portion of the integrated circuit die **104**, not including sensing surface **106**, is encapsulated in a plastic or epoxy material **112** protecting the integrated circuit and wire bonds **114** connecting the integrated circuit die **104** to pins **116** formed from a portion of the lead frame **108**. Plastic or epoxy material **112** is formed by molding in accordance with the known art. A lead frame strip having several lead frames, each bearing an integrated circuit die and wire bonds connecting the integrated circuit die to the respective lead frame, is mounted on the mold with the integrated circuit die and wire bonds received by a mold cavity. The mold cavity includes surfaces contacting the sensing surface **106** of each integrated circuit die to prevent plastic or epoxy encapsulating material from adhering to the sensing surface. Plastic or epoxy material is then formed to encapsulate portions of the integrated circuit die not contacted by the mold surface, the wire bonds, and the surfaces of the lead frame overlying the mold cavity.

Also formed from a portion of lead frame **108** is an electrostatic discharge ring. The electrostatic discharge ring is formed by folding a portion of the lead frame **108** from the bottom of integrated circuit die **104** and plastic or epoxy material **112** up around the sides and over a peripheral portion of the top surface. Lead frame **108** is stamped with portions

preformed for folding over the sides and top during lead frame trim and form operations.

After packaging is completed, lead frame **108** includes a first portion **108a** underlying the integrated circuit die **104**, plastic or epoxy material **112**, and bond wires **114**. Much of first portion **108a** comprises a die paddle to which the integrated circuit die is affixed. Second portions **108b** along the sides of the integrated circuit package **102**, and third portions **108c** overlying a peripheral portion of an upper surface of integrated circuit package **102**. (Part of the overlying peripheral portion **108c** is depicted as broken-away on the left side of **Figure 1A** to depict pins **114**). Pins **116** are also formed from portions of the stamped lead frame **108**, but are, for the most part, separated from lead frame **108** during packaging trim and form operations and are held in place by plastic or epoxy material **112**. At least one pin **116a** (best seen in **Figure 1D**) remains connected to lead frame **108**, serving as a ground connection for the electrostatic discharge ring. The remaining pins are, after fabrication of integrated circuit package **102** is complete, electrically and physically isolated from lead frame **108** and pin **116a**, and may instead be electrically connected to the integrated circuit die **104** via bond wires **114**.

As illustrated in **Figure 1E**, the electrostatic discharge ring formed by the folded portions of lead frame **108b** and **108c** may extend along a peripheral edge **118a** of packaged integrated circuit **102** which is opposite pins **116**, with an opening

through the folded lead frame portions **108b** and **108c** allowing access to pins **116** for an external connector. Alternatively, the electrostatic discharge ring may contain a broken region along a peripheral edge **118b** opposite pins **116**. The required length of the pins which must remain exposed for a connector, the thickness of the integrated circuit **104** and plastic or epoxy material **112**, and other design considerations may affect whether the electrostatic discharge ring extends along a complete circumference of the packaged integrated circuit **102**.

Referring to **Figures 2A** through **2D**, various views of alternative designs for a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention are illustrated. While the embodiment of **Figure 1A** through **1E** included straight pins for connection of the packaged integrated circuit to an external connector receiving the pins, the embodiments of **Figures 2A** through **2D** include gull wing leads for mounting the packaged integrated circuit on a printed circuit board with soldered connections.

Figure 2A is a plan view of one alternative embodiment of a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions, while **Figure 2B** is a cross-sectional view of the same alternative embodiment taken at section lines **B-B**. Packaged integrated circuit **202a** includes an integrated circuit die **204** containing sensor circuitry and including a sensor surface **206**. Integrated circuit die **204** is affixed on a bottom surface to lead frame **208** by an adhesive **210**, and is partially

encapsulated on remaining surfaces by a plastic or epoxy material **212**, but not over sensing surface **206**. Plastic or epoxy material **212** also encapsulates bond wires **214** electrically connecting the integrated circuit die **204** to the leads **216**.

While the embodiment of **Figures 1A** through **1E** included (or could have included) an electrostatic discharge ring along an entire circumference of an upper peripheral edge of the packaged integrated circuit, the length of lead frame material required to form gull wing leads **216** and the thin dimension of the packaged integrated circuit in the embodiment of **Figures 2A** through **2D** prevents the electrostatic discharge ring from extending all the way around the packaged integrated circuit **202a**. Nonetheless, portions **208b** and **208c** of the lead frame **208** are folded up around the sides and over a peripheral top portion of packaged integrated circuit **202a** wherever possible to form an incomplete "ring" connected to ground and dissipating electrostatic charge when contacted by a human finger.

Figure 2C is a plan view of another alternative embodiment of a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions, while **Figure 2D** is a cross-sectional view of that alternative embodiment taken at section lines **C-C**. While the embodiment shown in **Figures 2A** and **2B** includes wire bonds **214** within plastic or epoxy material **212** on only one side, the packaged integrated circuit **202b** of **Figures 2C** and **2D** includes bond wires **214** encapsulated by plastic or epoxy

material **212** on both sides. Either structure may be formed in the present invention.

With reference now to **Figures 3A** and **3B**, plan views of lead frame strips utilized in forming a packaged surface mount integrated circuit having an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention are depicted. The uncut lead frame strip **300** depicted in both **Figure 3A** and **3B** contains a plurality of lead frames with integral electrostatic discharge ring portions for packaging integrated circuits. Each lead frame includes a die paddle **302** to which the integrated circuit die is affixed. Sections **304** of the lead frame will form the electrostatic discharge ring after being folded up around the sides and over an upper peripheral portion of the integrated circuit structure being packaged by the lead frame.

Other portions **306** of the lead frame will form the pins or leads of the finished integrated circuit package and will be separated from the remainder of the lead frame during trim and form operations, except for one or more pins or leads providing a grounding connection to the lead frame and electrostatic discharge ring. The pins or leads formed from portions **306** will be held in place by plastic or epoxy encapsulating material molded around at least parts of the integrated circuit die mounted on the leadframe, and will be electrically connected to the integrated circuit by bond wires within the plastic or epoxy encapsulating material. Shorting bars **308**, containing "tooling" or alignment holes **310**, provide structural support for the lead frame and will be removed during lead frame trim and form operations.

During lead frame trim and form operations, sections of each lead frames will be folded along the dashed fold lines **312** depicted in **Figure 3B**. These sections will be folded up around the sides and over a peripheral upper surface of the integrated circuit package to form the electrostatic discharge ring. These sections remain physically and electrically connected to the lead frame die paddle on which the integrated circuit die is mounted, and are connected through the lead frame to a grounding connection. When a human finger touches the electrostatic discharge ring formed from these folded section in contacting the sensing surface of the packaged integrated circuit, any electrostatic charge is dissipated to ground by the electrostatic discharge ring.

Referring to **Figures 4A-4C**, various views of a narrow-strip packaged integrated circuit with gull-wing leads and an integral electrostatic discharge ring formed from lead frame portions in accordance with a preferred embodiment of the present invention are illustrated. **Figure 4A** shows a plan view of narrow-strip packaged integrated circuit **402**, while **Figure 4B** shows a side view and **Figure 4C** shows a cross-sectional view taken at section lines **D-D**. Packaged integrated circuit **402** includes an integrated circuit die **404** having a sensing surface **406** mounted on a lead frame **408** with an adhesive **410**. Plastic or epoxy material **412** encapsulates portions of integrated circuit die **404** other than sensing surface **406** and wire bonds **414** connecting integrated circuit die **404** to leads **416**. Leads **416** are formed from portions of lead frame **408**, but are separated from lead frame **408** during lead frame trim and form operations, except for one lead

providing a grounding connection for lead frame **408** and the electrostatic discharge ring.

Portions **408b** and **408c** of the lead frame **408** projecting from a bottom portion **408a** are folded up around the sides of the package (portions **408c**) and bent over to be level with an upper surface of plastic or epoxy material **412**. These portions **408b** and **408c** form an electrostatic discharge "ring" for packaged integrated circuit **402** by providing a low resistance path to ground. Because of the narrowness of the package and the required length of leads **416**, the electrostatic discharge "ring" is formed only along the long edges of package **402**, and not on the ends. However, the portions **408b** and **408c** of lead frame **408** which form the electrostatic discharge protection are close enough to the exposed sensing surface of the packaged integrated circuit to be contacted when a finger touches the sensing surface.

In the present invention, an electrostatic discharge ring for packaged integrated circuits is integrally formed from a portion functions by creating a path for accumulated electric charge to flow from the human finger or other item touching the packaged device to ground. Because the electrostatic discharge ring presents a low resistance path relative to the sensor area and the packaging materials, the electrostatic discharge ring serves as the preferred path from a region of high charge to a grounded region. Therefore, when a user of the sensor touches the sensor area, the user's finger will contact or come in close proximity with the electrostatic discharge ring, at which time any excess charge accumulated on the user will pass through the electrostatic discharge ring to ground, protecting the integrated circuit within the package.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of providing electrostatic discharge protection for an integrated circuit, comprising:

mounting an integrated circuit die on a lead frame;

encapsulating at least part of the integrated circuit die with a plastic or epoxy material; and

folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material.

2. The method of claim 1, further comprising:

connecting the portion of the lead frame folded around the sides of the encapsulated integrated circuit die and over or adjacent to the peripheral upper surface of the plastic or epoxy material to a ground voltage.

3. The method of claim 1, wherein the step of encapsulating at least part of the integrated circuit die with a plastic or epoxy material further comprising:

after mounting the integrated circuit die on the lead frame, encapsulating exposed surfaces of the integrated circuit die except for a sensing surface; and

encapsulating wire bonds connecting the integrated circuit die to portions of the lead frame.

4. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding portions of the lead frame around each side of the encapsulated integrated circuit die.

5. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a first side of the encapsulated integrated circuit die, wherein the first portion includes an opening providing access for a connector to pins electrically connected to the integrated circuit die.

6. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding portions of the lead frame around edges of the encapsulated integrated circuit die not including leads electrically connected to the integrated circuit die.

7. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a side of the encapsulated integrated circuit die; and

folding a second portion of the lead frame extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die.

8. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral

upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a side of the encapsulated integrated circuit die; and

folding a second portion of the lead frame extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

9. An integrated circuit package, comprising:

an integrated circuit die mounted on a lead frame; and

a plastic or epoxy material encapsulating at least part of the integrated circuit die,

wherein a portion of the lead frame is folded around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material.

10. The integrated circuit package of claim 9, further comprising:

a connection between a ground voltage and the portion of the lead frame folded around the sides of the encapsulated integrated circuit die and over or adjacent to the peripheral upper surface of the plastic or epoxy material.

11. The integrated circuit package of claim 9, wherein the plastic or epoxy material encapsulates exposed surfaces of the integrated circuit die except for a sensing surface and wire bonds connecting the integrated circuit die to portions of the lead frame.

12. The integrated circuit package of claim 9, wherein portions of the lead frame are folded around each side of the encapsulated integrated circuit die.

13. The integrated circuit package of claim 9, wherein a first portion of the lead frame folded around a first side of the encapsulated integrated circuit die includes an opening providing access for a connector to pins electrically connected to the integrated circuit die.

14. The integrated circuit package of claim 9, wherein portions of the lead frame are folded only around edges of the

encapsulated integrated circuit die not including leads electrically connected to the integrated circuit die.

15. The integrated circuit package of claim 9, wherein:

a first portion of the lead frame is folded around a side of the encapsulated integrated circuit die; and

a second portion of the lead frame extending from the first portion is folded over a peripheral upper surface of the encapsulated integrated circuit die.

16. The integrated circuit package of claim 9, wherein:

a first portion of the lead frame is folded around a side of the encapsulated integrated circuit die; and

a second portion of the lead frame extending from the first portion is folded adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

17. An integrated circuit package, comprising:

a lead frame including a die paddle and portions extending from the die paddle;

an integrated circuit die mounted on the die paddle;

a plastic or epoxy material encapsulating exposed surfaces of the integrated circuit die except for a sensing surface,

wherein the portions of the lead frame extending from the die paddle are folded around sides of the encapsulated integrated circuit die and over or adjacent to peripheral upper surfaces of the encapsulated integrated circuit die.

18. The integrated circuit package of claim 17, wherein the lead frame includes pins or leads and the portions extending from the die paddle include openings around the pins or leads.

19. The integrated circuit package of claim 17, wherein the lead frame includes pins or leads and the portions extending from the die paddle project from peripheral edges of the die paddle not adjacent to the pins or leads.

20. A lead frame strip for an integrated circuit package, comprising:

at least one lead frame, the lead frame including:

a die paddle on which an integrated circuit will be mounted;

a plurality of structures which will be formed into pins or leads for the integrated circuit package; and

portions extending from the die paddle which will be folded around sides of the integrated circuit package and over or adjacent to a peripheral upper surface of the integrated circuit package to form an electrostatic discharge ring.

SURFACE MOUNT PACKAGE WITH INTEGRAL ELECTRO-STATIC CHARGE DISSIPATING RING USING LEAD FRAME AS ESD DEVICE

ABSTRACT OF THE DISCLOSURE

In a packaged integrated circuit, electrostatic discharge protection is provided by portions of a lead frame on which the integrated circuit is mounted. The lead frame includes a die paddle on which an integrated circuit die is mounted, with plastic or epoxy material encapsulating exposed surfaces of the integrated circuit die except for a sensing surface, and supporting pins or leads formed from the lead frame. Portions of the lead frame extending from the die paddle are folded around sides of the encapsulated integrated circuit die and over, or adjacent to and level with, a peripheral upper surface of the encapsulated integrated circuit die to form an electrostatic discharge ring. The lead frame portions folded around the integrated circuit package are connected to ground through a ground pin, so that charge on a human finger touching the electrostatic discharge ring is dissipated to ground before the finger contacts a sensing surface of the integrated circuit. The portions of the lead frame which are folded around the encapsulated integrated circuit die may extend only around sides or side regions of the integrated circuit package not including pins or leads or, alternatively, may extend around all sides of the integrated circuit package and have openings where side regions of the integrated circuit package includes pins or leads.

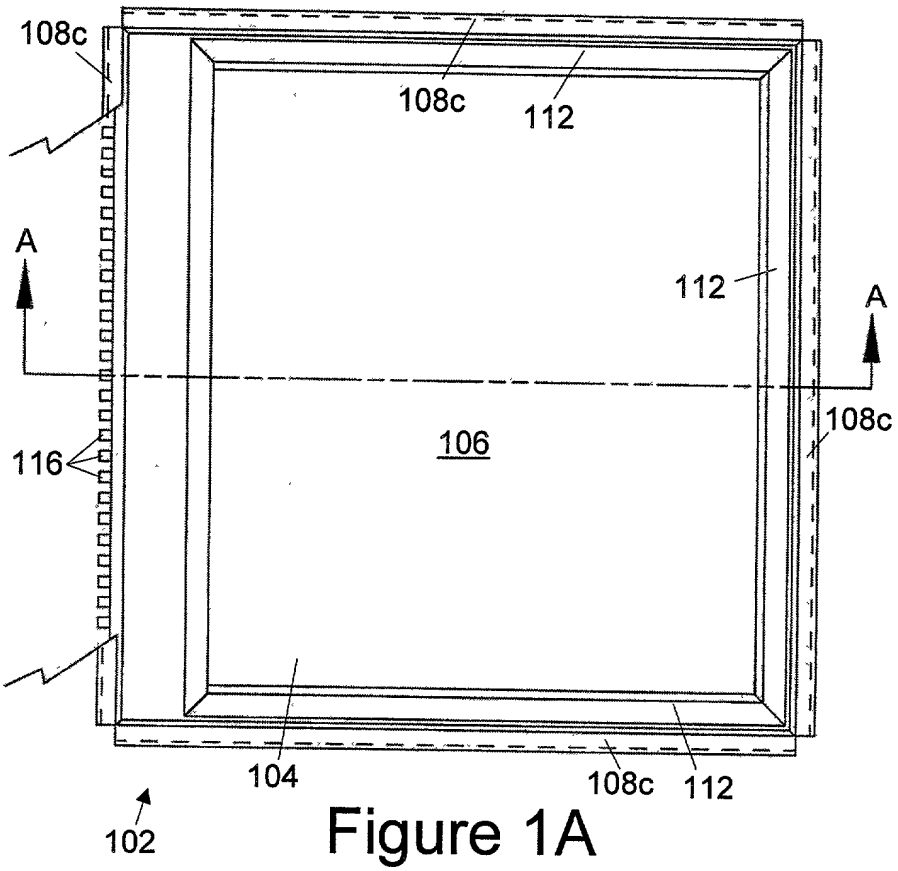

Figure 1A

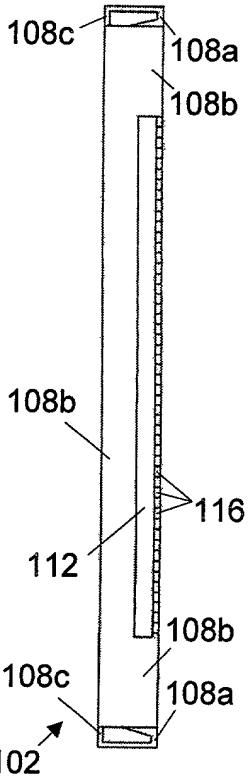

Figure 1B

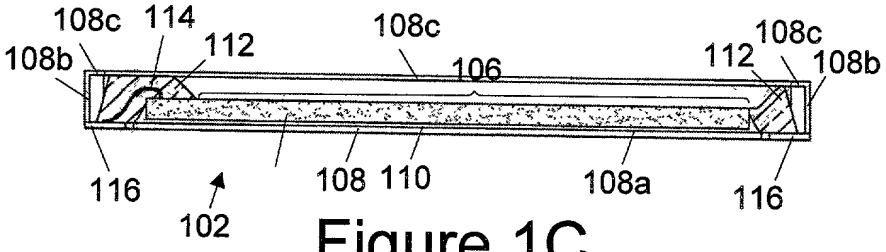

Figure 1C

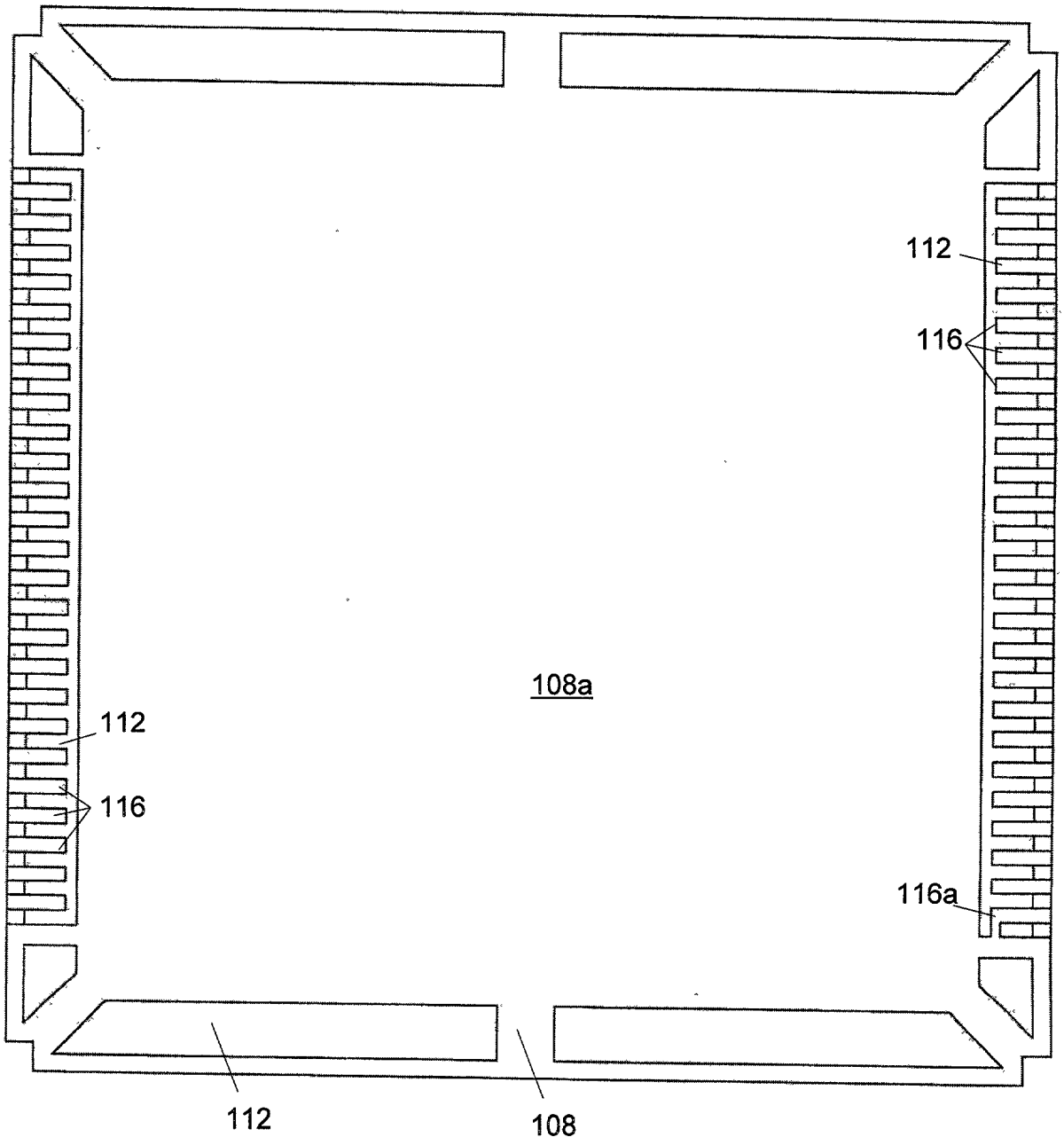

Figure 1D

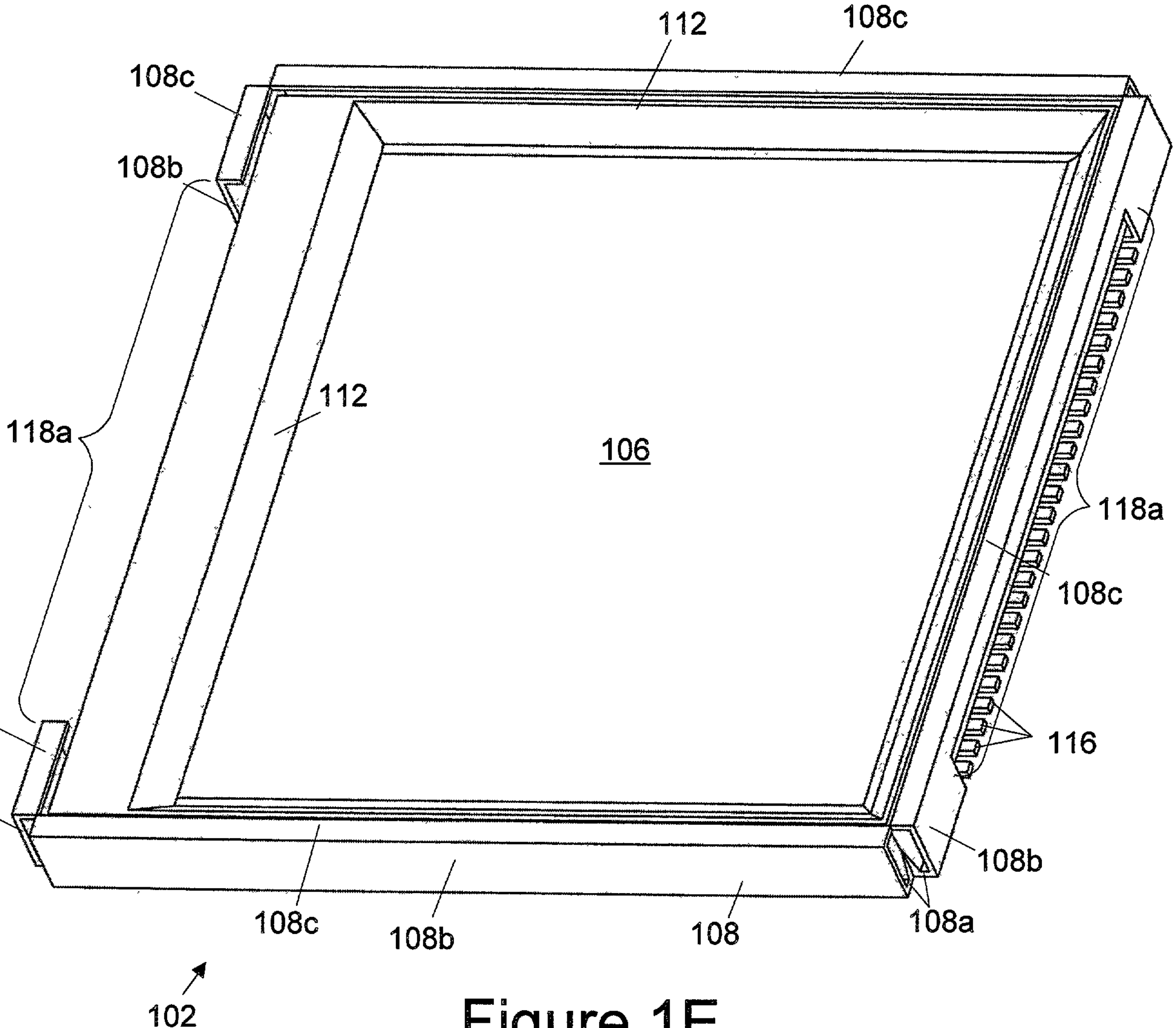
112
108c
108c
108b
118a
112
106
118a
108c
108c
116
108b
108b
108c
108b
108
108a
102

Figure 1E

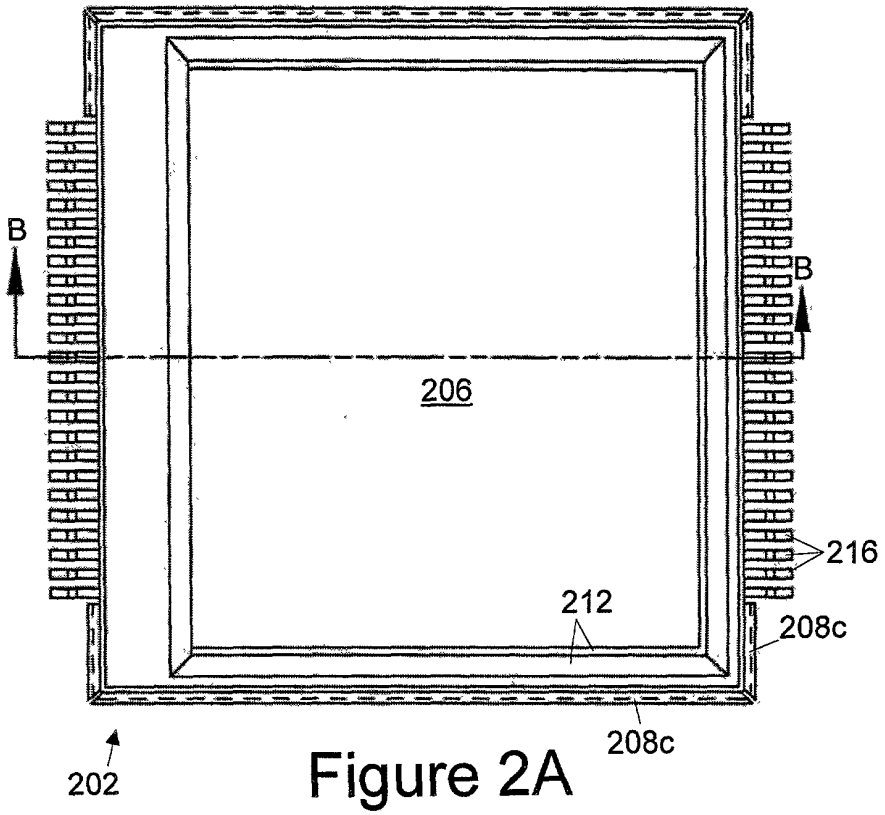

Figure 2A

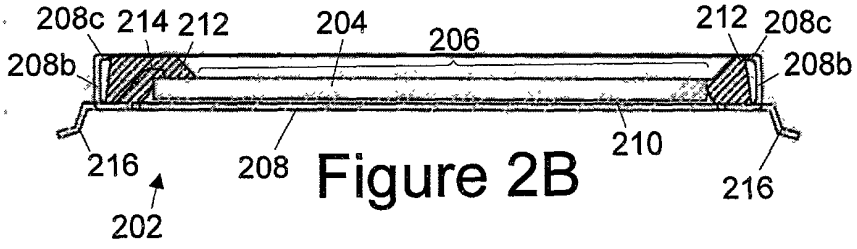

Figure 2B

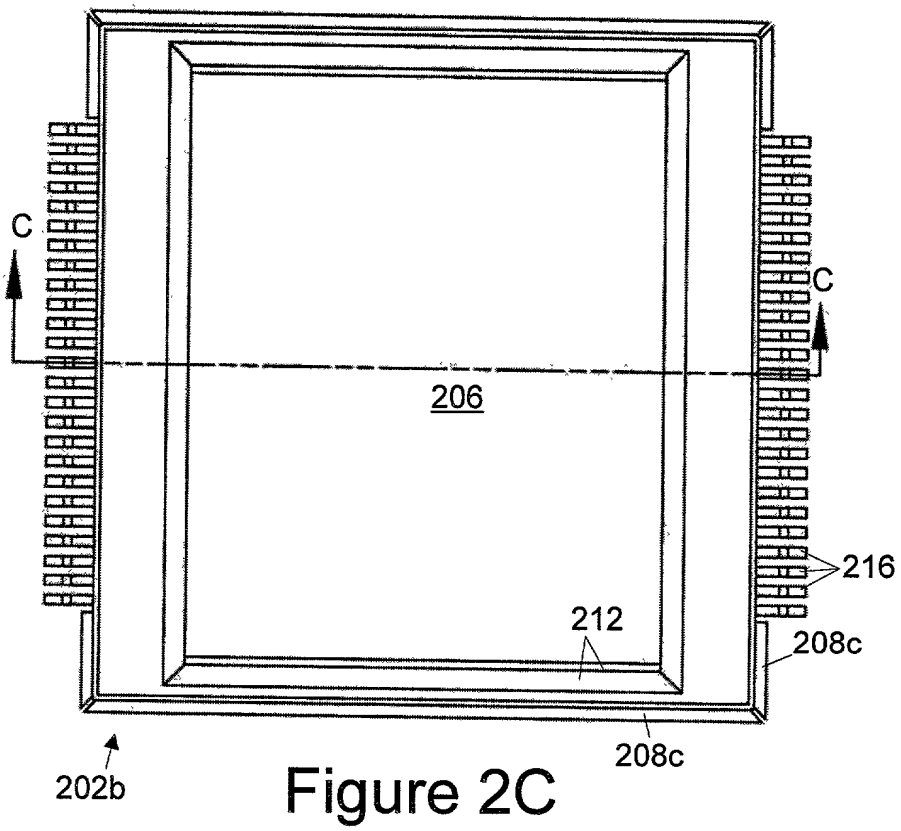

Figure 2C

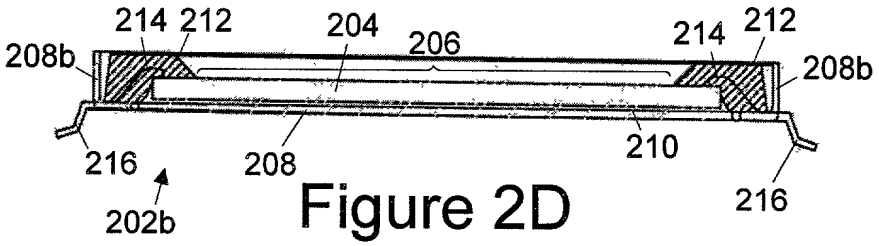

Figure 2D

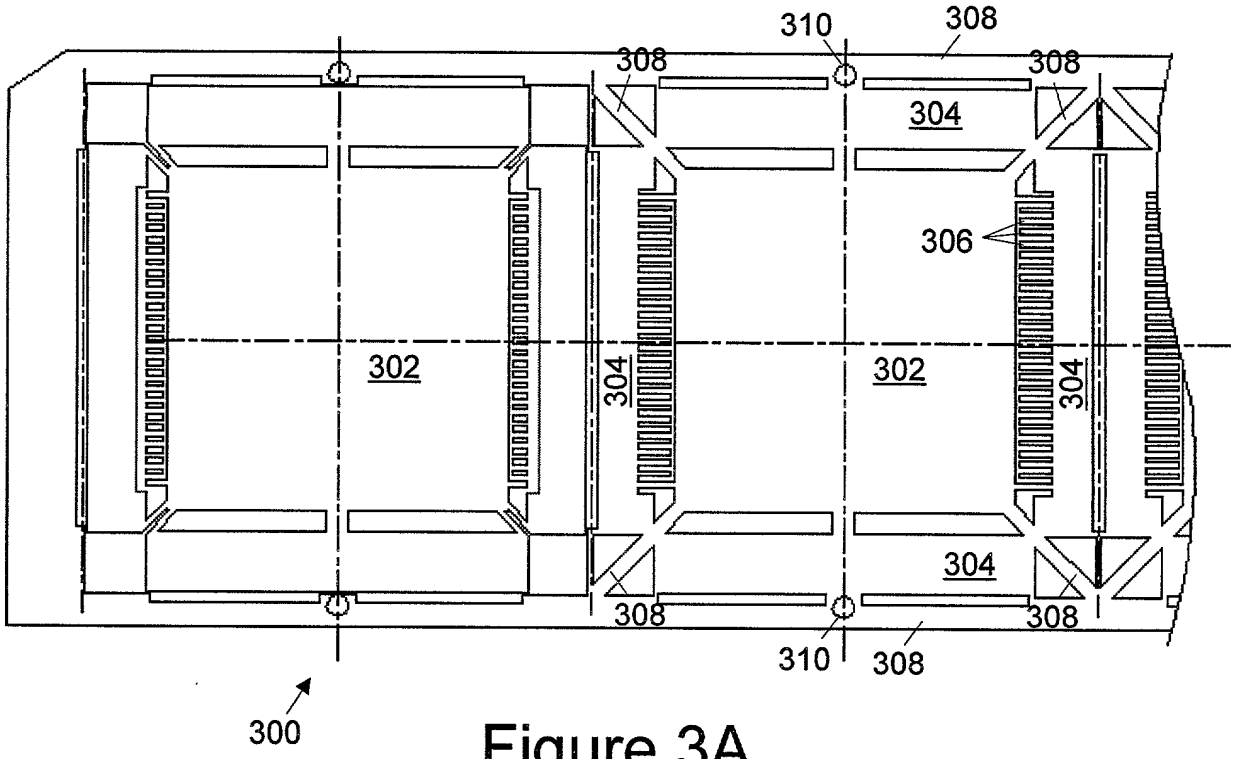

Figure 3A

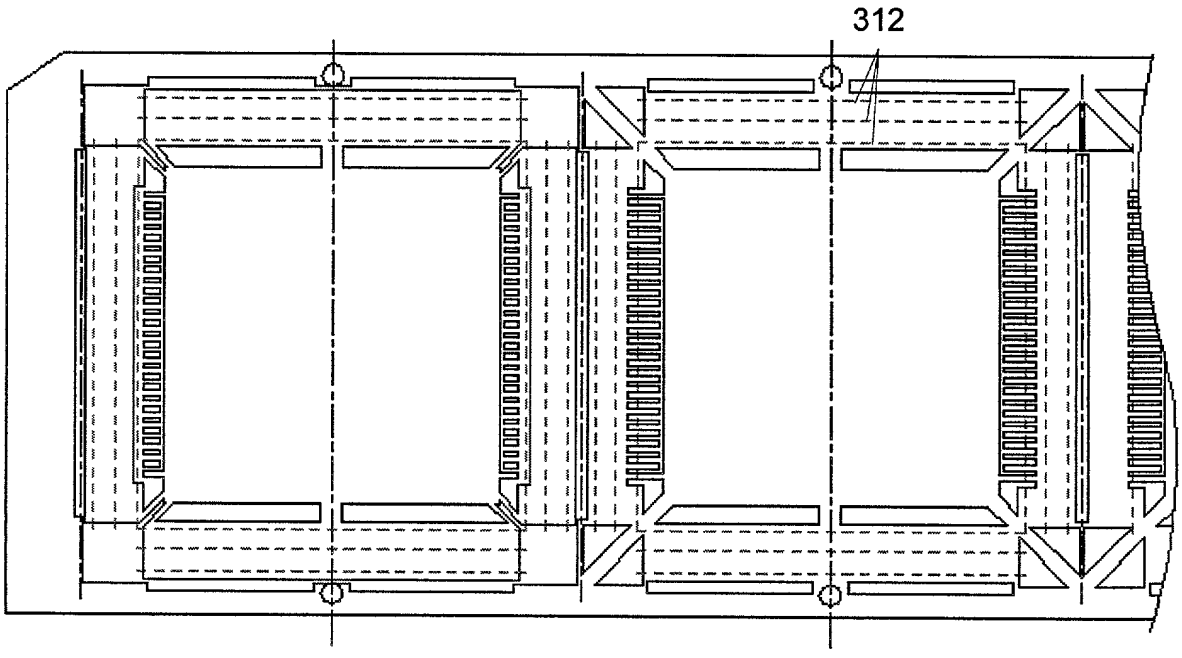

Figure 3B

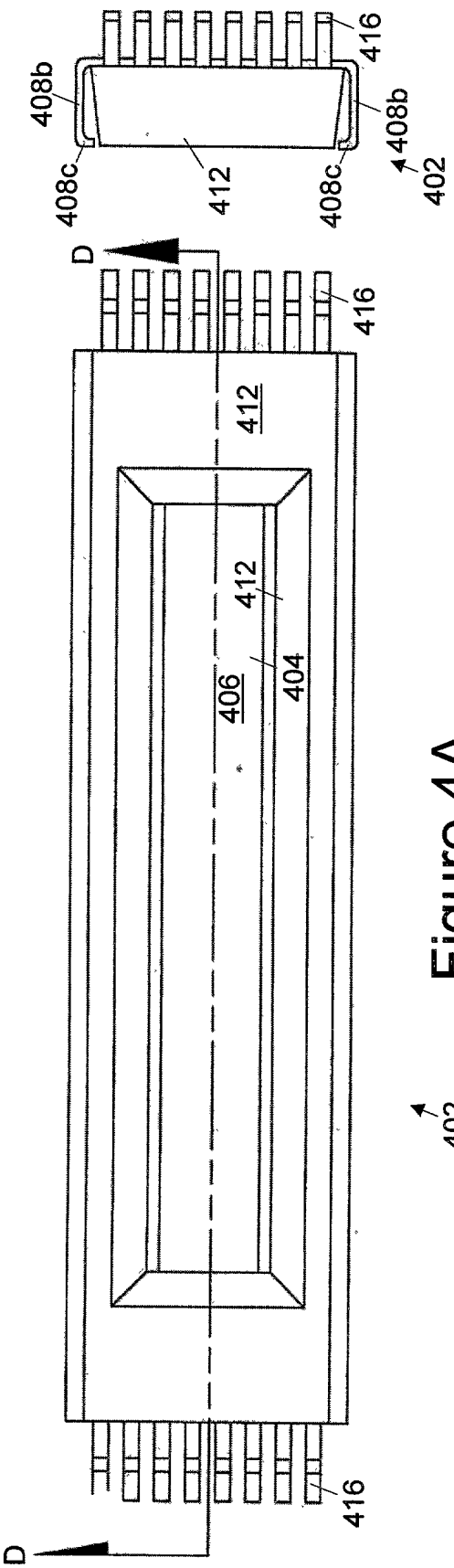

Figure 4A

Figure 4B

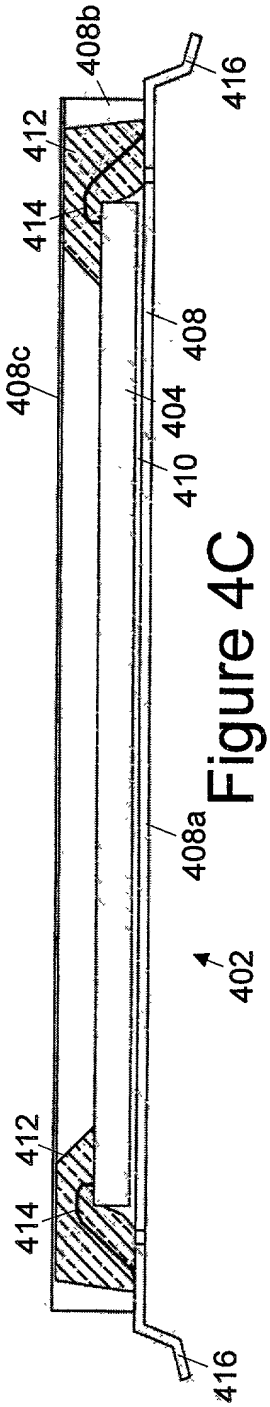

Figure 4C

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

SURFACE MOUNT PACKAGE WITH INTEGRAL ELECTRO-STATIC CHARGE DISSIPATING RING USING LEAD FRAME AS ESD DEVICE

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s): Priority Claimed

(Number)	(Country)	(Day/Month/Year)	___ Yes___ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial #)	(Filing Date)	(Status)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Docket No. 00-C-016

I hereby appoint Theodore E. Galanthay, Reg. No. 24,122; Lisa K. Jorgenson, Reg. No. 34,845; Robert D. McCutcheon, Reg. No. 38,717; Mario Donato, Reg. No. 37,817; James E. Bradley, Reg. 27,536; Charles D. Gunter, Jr., Reg. No. 29,386; Andrew J. Dillon, Reg. No. 29,634; Jack V. Musgrove, Reg. No. 31,986; Daniel E. Venglarik, Reg. No. 39,409; Brian F. Russell, Reg. No. 40,796; Matthew W. Baca, Reg. No. 42,277; and Antony P. Ng, Reg. No. 43,427 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

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